REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is respectfully requested.

The Notice of Allowance was vacated in view of this new Action and the prosecution of the case was reopened.

The Examiner objects to claims 2-13, 18, 20-24 because the term "ADC" should be inserted after the phrase "successive approximation". Applicant's have inserted the term in all of the claims suggested by the Examiner except 18, and 20-23. In view of the fact that these are method claims, Applicant's have instead inserted --analog to digital conversion--.

The Examiner rejects claims 18 and 24 under 35 U.S.C. § 102(b) as being anticipated by Watson et al. The Examiner specifically refers to FIGURE 3 of this reference.

We can not agree. Watson utilizes a separate analog to digital converter 24 for each bit in the conversion. In Watson, the comparator makes a comparison between the conversion between the input signal to a digital signal and then back to an analog signal, amplifies the difference and then passes this on to the next stage. Therefore, one ADC is required for each bit of resolution.

In sharp contrast, the present invention only utilizes a single multi-bit ADC which functions as a comparator until the amplified different signal is within the range of the ADC, thus reutilizing the same circuitry for generating all of the bits. Claims 18 and 24 have been amended in this respect.

The Examiner rejects claims 18-24 under 35 U.S.C. §102(b) as being anticipated by Hollister. The Examiner specifically refers to Figures 1, 5 and 6 of Hollister.

We can not agree. The Examiner has stated that the amplifier (22) receives an output of the difference generated by the summer (30). However, the output of the summer (30) is input to the memory (32) and does not provide the different signal from the summer (30) to the amplifier (22) as can clearly be seen by looking at FIGURE 1. The Examiner then refers to a multi-bit ADC (24), although, clearly element (24) is labeled a peak detector. Accordingly, Applicant's believe that the Examiner meant to refer to ADC (26). Which is coupled to the output of amplifier (22) but does not amplify the different signal from adder (30) rather takes the signal which is generated by sampling head (16) through the sampling preamps, attenuator (20) into the amplifier (22) through the peak detector (24) and then into the ADC. Accordingly, the elements do not line up as the Examiner has stated and thus, an '102 rejection must fail.

The Examiner rejects claims 2-11, 13-23 as being unpatentable under 35 U.S.C. § 103(a) over Watson et al. in view of Burns. In view of the fact that the Claim 24 has been shown to be patentable distinct from Watson et al., combining Watson et al. with Burns does not render the claims unpatentable.

The Examiner has found that Claim 12 is objected to as being unpatentable dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations to the base claim and the intervening claims. Claim 12 is dependent on Claim 24. the patentability of Claim 24 having been shown above, Claim 12 is patentable for the same reasons.

Accordingly, Applicants believe the Application, as amended, is in condition for allowance, and such action is respectfully requested.

Respectfully submitted,

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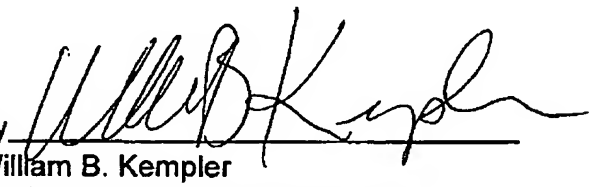
By 

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